WHAT IS CLAIMED IS:

1. A data input device of a DDR SDRAM comprising:

a clock pulse generator for receiving an internal clock, which operates in a write mode, and outputting a data-in-strobe signal that is a first control signal;

a first data buffer an operation of which is controlled by the data-in-strobe signal and an output line of which corresponds to a first global input/output line of the DDR SDRAM; and

a second data buffer an operation of which is controlled by the data-in-strobe signal and an output line of which corresponds to a second global input/output line of the DDR SDRAM;.

wherein if a second control signal is in a low level, first data is directly applied to the first data buffer to be transferred to the first global input/output line, and second data is directly applied to the second data buffer to be transferred to the second global input/output line; and

wherein if the second control signal is in a high level, the first data is directly applied to the second data buffer to be transferred to the second global input/output line, and the second data is directly applied to the first data buffer to be transferred to the first global input/output line.

2. The data input device of claim 1, wherein the second control signal outputs a low level if the least significant bit (LSB) of a column address applied in the write mode is "0", and outputs a high level if the LSB of the column address is "1".

3. The data input device of claim 1, wherein the first data buffer selectively receives the first data or the second data through one input terminal.

4. The data input device of claim 1, wherein the first data buffer selectively receives the first data or the second data through two input terminals.